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# PATENT ABSTRACTS OF JAPAN

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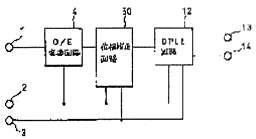
## (54) SYNCHRONIZATION CONTROL SYSTEM

(57)Abstract:

PROBLEM TO BE SOLVED: To prevent the situation that it takes time for phase comparison of a DPLL circuit, pull-in time is not converged within the preamble of a data string and the head part of data causes a code error.

SOLUTION: This system is provided with a phase correction circuit 50 for detecting the phase deviation of reset input signals synchronized with a reference clock and reception data and delaying the reception data so as to correct the phase deviation. By correcting the phase deviation due to asynchronization before re-timing by the DPLL circuit 12, the pull-in time is shortened. Thus, since the pull-in time is converged within the preamble of the data string, the head part of the data does not cause the code error.



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## CLAIMS

[Claim(s)]
[Claim 1]It is a synchronous control system which has a DPLL circuit which synchronizes with an internal clock received data received from the outside, A synchronous control system having the phase compensator which amends a phase shift of data which should be inputted into said DPLL circuit, inputting data after this phase shift amendment into said DPLL circuit, and performing phase simulation level luffing motion.
[Claim 2]A capacitative element by which only time when said voltage converting means is equivalent to said phase contrast is charged, A peak detector which detects a peak value of charge voltages of this capacitative element, and a sample hold circuit which samples and holds this peak value with sampling clocks in sync with said clock are included, The synchronous control system according to claim 1 controlling a time delay of said delay means according to output voltage of this sample hold circuit.
[Claim 3]The synchronous control system comprising according to claim 1 or 2:
A voltage converting means from which said phase compensator changes phase contrast of said received data and said internal clock into voltage.
A delay means which a time delay is controlled [ delay means ] according to this changed voltage, and delays said received data.

[Claim 4]The synchronous control system comprising according to claim 3:
A delay circuit which has a time delay equivalent to conversion process time according [ said delay means ] to said voltage converting means.
An integration circuit which integrates with said received data with a damping time constant controlled according to voltage changed by said voltage converting means.

[Claim 5]The synchronous control system comprising according to claim 4:

A capacitative element in which an electric charge is accumulated by voltage from which said integration circuit was changed by said voltage converting means.
A resistance element which constitutes a time constant circuit with this capacitative element.

[Claim 6]The synchronous control system according to any one of claims 1 to 5 integrating said phase compensator to said DPLL circuit and one.

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[Translation done.]

## DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]Especially this invention relates to the synchronous control system which has a DPLL circuit which synchronizes with an internal clock the received data received from the outside about a synchronous control system.

[0002]

[Description of the Prior Art]The data level luffing motion of the burst data receiving system using the timing sampling procedure by the DPLL (Digital Phase Locked Loop) circuit in conventional technology is explained. The composition of an example of the synchronous control system by conventional technology is shown in drawing 7. If the figure is referred to, in the conventional synchronous control system, it is constituted including the light / electrical conversion circuit 4 (it abbreviates to an O/E conversion circuit hereafter) which changes an optical reception signal into an electrical signal, and DPLL circuit 12 which synchronizes the electrical signal after this conversion with a reference clock. And the optical reception signal input terminal 1 and the reset signal input terminal 2 are respectively connected to the input of the O/E conversion circuit 4, and the output, the reset signal input terminal 2, and the reference clock input terminal 3 of the O/E conversion circuit 4 are respectively connected to the input of DPLL circuit 12. The output clock of DPLL circuit 12 is connected to the output clock terminal 13, and data output is connected to the data output terminal 14.

[0003]DPLL circuit 12 has two or more kinds of counting-down circuits inside.
It is a circuit which chooses and uses two or more of these counting-down circuits, and constitutes well-known PLL.
By constituting PLL, retiming processing which synchronizes the signal inputted with a reference clock is performed.

[0004]The timing chart of the synchronous control system of drawing 7 of operation is shown in

drawing 8. Here, a reset input signal and a reference clock signal shall be in a synchronous state, and the optical reception signal and reset input signal which are inputted shall have them in an asynchronous state. The Motonobu item received shall be the composition that the preamble data P is added to the head of burst data.

[0005]First, the Motonobu item inputted into the optical received input terminal 1 is changed and outputted to an electrical signal in the O/E conversion circuit 4. In the figure, the inputted preamble data P of the Motonobu item is expressed as "A", "B", "C", and "D", and data required after this preamble data P is added.

[0006]Here, in order to identify the data transmitted in the state of a gear-tooth omission, it is necessary to initialize a circuit by a non-signal state. For this reason, the reset signal is given between the burst data row and the burst data row. In this case, the time interval of data rows is beforehand measured at the time of initial setting of a system, and the cycle of a reset signal is determined based on this measurement result. By carrying out like this, a data row and a reset signal do not lap, and timing adjustment is made so that a reset signal may exist between data rows.

[0007]The internal reference clock signal of a reception side circuit is inputted into the reference clock input terminal 3. In order to take the synchronization of the electrical signal acquired from the O/E conversion circuit 4, in DPLL circuit 12, the phase comparison of a data signal and a reference clock signal is performed. By choosing the counting-down circuit that this phase comparison result becomes zero, the data output in sync with an output clock and this as shown in the figure is obtained.

[0008]Here, the phase comparison in DPLL circuit 12 is performed as follows. That is, from the reference clock signal inputted, the clock signal with which several kinds of phases differ is generated, and abundance detection of the phase relation of this clock signal and input data signal is carried out. And discernment of data chooses most the clock signal of the phase performed correctly. Retiming of the data is pierced and carried out with this selected clock. Time until a clock signal is chosen from this phase-comparison start draws, and it becomes time.

[0009]Data is not normally identified until operation is stabilized from this level-luffing-motion start, but the signal mistaken in the output terminal of DPLL circuit 12 is outputted. If it is not completed by this state by within a time [ equivalent to the preamble data P ] as the whole receiving system, a digital error will occur in the data head part 120 (shadow area). When the phase comparison of the signal which the jitter has generated in the waveform after a light-receiving level is dramatically small and changes into an electrical signal is performed, this level-luffing-motion time tends to increase. The level-luffing-motion time produced at the time of this phase comparison can be divided roughly into time to adjust an asynchronous phase shift state and time to adjust the phase shift by a jitter.

[0010]As for a DPLL circuit, when a phase comparison becomes difficult and performs high-speed burst data communications so that access speed becomes high-speed, it is indispensable to perform level luffing motion at high speed. Therefore, inside a DPLL circuit, the circuitry of the phase comparison circuit which performs a phase comparison is complicated dramatically.

[0011]

[Problem(s) to be Solved by the Invention]It takes time to choose the clock of a phase with which it mentions above and discernment of data is correctly performed in conventional technology at the time of a phase comparison. It is remarkable about the signal which contained the jitter especially. As a result, if not completed by level-luffing-motion time by within a time [ equivalent to preamble data ], the head of data will start a digital error, and there is a fault of becoming erroneous transmission.

[0012]Time is required, in order for the time of one cycle to become short, and for the rate of the field which a jitter generates to also increase to an eye pattern and to identify data correctly, if access speed increases. Therefore, it becomes the circuitry which incorporated the policy which level-luffing-motion time does not increase. In this case, there is a fault that it is difficult to shorten this level luffing motion, and the circuitry inside DPLL is complicated, so that access speed becomes high-speed.

[0013]The art of shortening the phase level-luffing-motion time in a DPLL circuit also to JP,2-156726,A is indicated. This saves the operation data of the former synchronous state, is setting this as CPU and shortens the synchronous stabilization time at the time of the return after a fault occurrence. However, in this conventional technology, about the signal having contained the jitter, time for discernment of data to choose the clock of the phase performed correctly is taken, and cannot solve the fault mentioned above. To JP,61-240732,A, the rising characteristic (response) of the reference oscillator (crystal oscillator) of a power up is supervised, and the art of controlling and drawing the phase step width of PLL by adding a sampling circuit and an arithmetic circuit, and shortening time is indicated to it. However, about the signal which contained the jitter also in this conventional technology, it is not taken into consideration at all and, similarly the fault mentioned above cannot be solved.

[0014]Also in the burst data communications in which it was made in order that this invention might solve the fault of the conventional technology mentioned above, and the purpose contained the jitter at high speed, It is providing the synchronous control system which can oppress the increase in level-luffing-motion time, and can prevent digital-error generating of a head part, and also can prevent complication of a DPLL circuit.

[0015]

[Means for Solving the Problem]A synchronous control system by this invention is a synchronous control system which has a DPLL circuit which synchronizes with an internal

clock received data received from the outside, It has the phase compensator which amends a phase shift of data which should be inputted into said DPLL circuit, data after this phase shift amendment is inputted into said DPLL circuit, and it was made to perform phase simulation level luffing motion. A capacitative element by which only time when said voltage converting means is equivalent to said phase contrast is charged, A peak detector which detects a peak value of charge voltages of this capacitative element, and a sample hold circuit which samples and holds this peak value with sampling clocks in sync with said clock are included, A time delay of said delay means was controlled according to output voltage of this sample hold circuit. Said phase compensator includes a voltage converting means which changes phase contrast of said received data and said internal clock into voltage, and a delay means which a time delay is controlled [ delay means ] according to this changed voltage, and delays said received data. Said delay means includes a delay circuit which has a time delay equivalent to conversion process time by said voltage converting means, and an integration circuit which integrates with said received data with a damping time constant controlled according to voltage changed by said voltage converting means. Said integration circuit contains a capacitative element in which an electric charge is accumulated by voltage changed by said voltage converting means, and a resistance element which constitutes a time constant circuit with this capacitative element.

[0016]In short, this system has the phase compensator which amends a phase shift by asynchronous. This phase compensator detects a phase shift of a reset input signal and a received data signal, and it delays a received data signal so that that phase shift can be amended. Phase compensator is provided between an O/E conversion circuit and a DPLL circuit, and it has composition which amends a phase before an input of a DPLL circuit.

[0017]Phase compensator provided between an O/E conversion circuit and a DPLL circuit is a circuit which adjusts and amends an asynchronous phase shift state, it is passing through this circuit, and a phase shift of a data signal and a reset input signal which are inputted into a DPLL circuit is amended. Thereby, before being inputted into a DPLL circuit, a synchronization with a received data signal, a reference clock signal, and a reset signal can be taken, and a phase comparison for mainly amending a phase shift by a jitter is performed in a DPLL circuit. Inside a DPLL circuit, a function in particular for shortening level-luffing-motion time extremely is not needed.

[0018]

[Embodiment of the Invention]Next, one gestalt of operation of this invention is explained with reference to drawings. In each figure referred to in the following explanation, identical codes are given to other figures and equivalent portions.

[0019]Drawing 1 is a block diagram showing one gestalt of operation of the synchronous control system by this invention. When the figure is referred to, the point that this system

differs from the system of drawing 7 is a point that the phase compensator 50 is formed between the O/E conversion circuit 4 and DPLL circuit 12. That is, in this system, the optical reception signal input terminal 1 and the reset signal input terminal 2 are respectively connected to the input of the O/E conversion circuit 4, and the output, the reset signal input terminal 2, and the reference clock input terminal 3 of the O/E conversion circuit 4 are connected to the input of the complementary positive circuit 50 at least for each. And the output, the reset signal input terminal 2, and the reference clock input terminal 3 of the phase compensator 50 are respectively connected to the input of DPLL circuit 12. The output clock of DPLL circuit 12 is connected to the output clock terminal 13, and data output is connected to the data output terminal 14.

[0020]Next, operation of this system is explained, also referring to the time chart of drawing 2. Here, a reset signal and a reference clock signal shall be in a synchronous state, and the optical reception signal and reset signal which are inputted shall have them in an asynchronous state. The Motonobu item received shall be the composition that the preamble data P is added to the head of burst data.

[0021]First, the Motonobu item inputted into the optical received input terminal 1 is changed and outputted to an electrical signal in the O/E conversion circuit 4. In the figure, the inputted preamble data P of the Motonobu item is expressed as "A", "B", "C", and "D", and data required after this preamble data P is added.

[0022]Here, in order to identify the data transmitted in the state of a gear-tooth omission, it is necessary to initialize a circuit by a non-signal state. For this reason, the reset signal is given from the reset input terminal 2 between the burst data row and the burst data row. Having carried out point ** of the cycle of this reset signal is determined.

[0023]The internal reference clock signal of a reception side circuit is inputted into the reference clock input terminal 3.

[0024]First, in the O/E conversion circuit 4, the inputted optical reception signal is inputted into the phase compensator 50, light / after electrical conversion is carried out. And a delaying amount required of phase compensator 50 inside in order to detect the phase shift quantity by asynchronous [ of a received data signal and a reset signal ] and to double the phase shifted is detected, and it gives the input signal which was able to obtain delay of the part from the O/E conversion circuit 4. This amends the phase shift by asynchronous [ of the reset signal and received data signal in sync with a reference clock signal ]. The data signal which passed through the phase compensator 50 is inputted into DPLL circuit 12, and a phase comparison with a reference clock signal is performed.

[0025]Here, the phase comparison in DPLL circuit 12 is performed as follows as usual. That is, from the reference clock signal inputted, the clock signal with which several kinds of phases differ is generated, and abundance detection of the phase relation of this clock signal and an

input data signal is carried out. And discernment of data chooses most the clock signal of the phase performed correctly. Time until a clock signal is chosen from this phase-comparison start draws, and it becomes time.

[0026]In the time of this phase comparison, beforehand, since the phase shift by asynchronous is amended, comparison for mainly amending only the phase shift by a jitter is performed. Therefore, the time required in order to perform this phase correction and to carry out synchronous level luffing motion changes with jitter amounts. In drawing 2, the example which level luffing motion completed to within a time [ which is equivalent to "A" and "B" of the data head part 120 (shadow area) among the preamble data P ] is shown.

[0027]

[Example]Next, the example of this invention is described with reference to drawing 3. In the figure, the phase compensator 50 is constituted including the asynchronous phase shift detector circuit 6, the delaying amount/DC conversion circuit 10, the DC/DC converter 9, the sampling/hold circuit 8, the DC / delaying amount conversion circuit 7, and the delay circuit 5.

[0028]In the figure, the reset signal input terminal 2 is respectively connected to the reset input of the O/E conversion circuit 4, the asynchronous phase shift detector circuit 6, and DPLL circuit 12, and the reference clock terminal 3 is respectively connected to the clocked into of the asynchronous phase shift detector circuit 6 and DPLL circuit 12.

[0029]Next, the optical reception signal input terminal 1 is connected to the input of the O/E conversion circuit 4, the output of the O/E conversion circuit 4 is connected to the input of the delay circuit 5 and the asynchronous phase shift detector circuit 6, and the output of the delay circuit 5 is connected to the input of DC / delaying amount conversion circuit 7. The output of the asynchronous phase shift detector circuit 6 is connected to the input of a delaying amount / DC conversion circuit 10, and the output of the delaying amount / DC conversion circuit 10 is connected to the input of the DC/DC converter 9. The output of the DC/DC converter 9 is inputted into a sampling / hold circuit 8, and the output of the sampling / hold circuit 8 is connected to the control input of DC / delaying amount conversion circuit 7.

[0030]Here, the control signal output of the asynchronous phase shift detector circuit 6 is connected to the sampling-clocks input of a sampling / hold circuit 8. The output of DC / delaying amount conversion circuit 7 is connected to the input of DPLL circuit 12. The output clock of DPLL circuit 12 is connected to the output clock terminal 13, and the data output of DPLL circuit 12 is connected to the data output terminal 14.

[0031]The more detailed composition of each part of the asynchronous phase shift detector circuit 6 in drawing 3, the delaying amount/DC conversion circuit 10, and the DC / delaying amount conversion circuit 7 is shown in drawing 4. As shown in drawing 4 the asynchronous phase shift detector circuit 6, The monostable multivibrator circuit (it is hereafter called a monomulti vibrator circuit) 32 for detecting the standup position of a preamble data signal, It is

constituted including the inverter 40 and the monomulti vibrator circuit 35 for detecting the falling position of a reset signal (b). Between the power supply 38 and the ground 34, the resistance element 39 and the capacitative element 33 are formed, and the output pulse width of the monomulti vibrator circuit 32 is determined with these elements. Similarly, between the power supply 42 and the ground 37, the resistance element 43 and the capacitative element 36 are formed, and the output pulse width of the monomulti vibrator circuit 35 is determined with these elements.

[0032]The inverter 31 with which the asynchronous phase shift detector circuit 6 reverses the output of the monomulti vibrator circuit 32, AND circuit 30 which takes the logical product of this inverted output and the output of the monomulti vibrator circuit 35, This logical product output consists of standups of the reference clock including NOR circuit 28 which considers the D-flip-flop circuit 29, and this reversal Q output and the logical product output of AND circuit 30 as an input.

[0033]The delaying amount / DC conversion circuit 10 is constituted including the capacitative element 26 charged with the output of NOR circuit 28, and the peak detector 25 which detects the peak voltage by charge of this capacitative element 26. 27 is a ground.

[0034]The inverter 20 with which DC / delaying amount conversion circuit 7 was formed in the input stage, It is constituted including the inverter 23 formed in the output stage, the resistance element 45 and the capacitative element 21 which constitute an integration circuit, and the resistance 24 for charging the capacitative element 21 with the output of a sampling/hold circuit. 22 is a ground.

[0035]Operation of each part of drawing 4 is shown in the time chart of drawing 5. In drawing 5, the waveform of the portion of numerals (a) - (j) attached in drawing 4 is shown.

[0036]Here, a reset signal (b) and a reference clock signal (c) shall be in a synchronous state, and the optical input signal (a) and reset signal (b) to receive shall have them in an asynchronous state. As for the composition of the Motonobu item which receives, the preamble data P shall be added to the head of burst data.

[0037]First, the Motonobu item inputted into the optical received input terminal 1 is changed into an electrical signal in the O/E conversion circuit 4. Here, in a figure, the inputted preamble data of the Motonobu item shall be expressed as "A", "B", "C" and "E", "F", and "G", and data required after this preamble data shall be added.

[0038]In order to identify the data transmitted in the state of a gear-tooth omission, it is necessary to initialize a circuit by a non-signal state. For this reason, between a burst data row and a burst data row, a reset signal (b) is given from the reset input terminal 2. The reference clock signal (c) of a receiver is inputted into the reference clock input terminal 3.

[0039]In the O/E conversion circuit 4, the received optical data signal (a) is inputted into the phase compensator 50, light / after electrical conversion is carried out. In the asynchronous

phase shift detector circuit 6 of phase compensator 50 inside, the standup position of a preamble data signal and the falling position of a reset signal (b) are respectively detected using the monomulti vibrator circuits 32 and 35. The result of having detected the standup position of the preamble data signal is reversed, and a logical product is taken with the result and AND circuit 30 which detected the falling position of the reset signal. It uses as sampling clocks (g) which mention this signal later.

[0040]As a result of detecting the period from the falling position of this reset signal until a preamble data signal rises, it is processed by the D-flip-flop circuit 29 and NOR circuit 28. The signal for detecting time until the standup of a reference clock signal (c) comes from the standup of a preamble data signal by carrying out like this is acquired.

[0041]Here, the detected time serves as phase shift quantity by asynchronous, and it becomes a delaying amount for amending a phase. This signal is told to the delaying amount / DC conversion circuit 10 of the next step. In a delaying amount / DC conversion circuit 10, the capacitative element 26 is charged with the output signal of the asynchronous phase shift detector circuit 6, and the peak value of these charge voltages (d) is detected in the peak detection circuit 25. In this case, since full charge of the capacitative element 26 is carried out when phase shift quantity is large, the peak value of charge voltages (d) becomes large. On the contrary, when phase shift quantity is small, full charge of the capacitative element 26 is not carried out, but the peak value of charge voltages (d) becomes small. Thus, the delaying amount for amending a phase is changed into the DC voltage of V1 and V2 by detecting a peak value. This changed DC signal is an output signal (e) of a delaying amount / DC conversion circuit 10.

[0042]Next, with the DC/DC converter 9, a DC signal is increased N times and turns into a signal (f) of V1xN and V2xN. Thus, increasing N times, the output signal (e) of a delaying amount / DC conversion circuit 10 is a minute pressure value.

It is for using a pressure value required to give an electric charge to the capacitative element 21 mentioned later.

[0043]In a sampling / hold circuit 8, the sampling clocks (g) outputted from the asynchronous phase shift detector circuit 6 perform sampling/hold operation of a signal (f). And between 1 bursts, the sampled DC signal is held and is stabilized. A DC signal (h) is outputted from this sampling / hold circuit 8. Sampling clocks (g) are signals which change whenever a burst signal is inputted.

[0044]Using the DC signal (h) outputted from a sampling / hold circuit 8, by DC / delaying amount conversion circuit 7, an electric charge is given to the capacitative element 21 and the standup of an input signal and falling are adjusted to the threshold of the inverter circuit 23. You make it delayed by carrying out like this so that the phase shift according the input signal

inputted via the delay circuit 5 to asynchronous may be amended. Thereby, a data signal (j) is outputted from DC / delaying amount conversion circuit 7.

[0045]Here, the delaying amount of the delay circuit 5 is set as the amount of absolute delay in the asynchronous phase shift detector circuit 6, the delaying amount/DC conversion circuit 10, the DC/DC converter 9, and the sampling/hold circuit 8. That is, the phase contrast of an optical data signal (a) and data signal (i) after delay by the delay circuit 5 is equivalent to the delaying amount.

[0046]The data signal (j) acquired from DC / delaying amount conversion circuit 7, After being inputted into DPLL circuit 12, the result of having performed the phase comparison of a preamble data signal and a reference clock signal, and having performed retiming to the output clock terminal 13 and the data output terminal 14 is obtained as usual using the clock with which several kinds of phases differ.

[0047]Next, other gestalten of operation of this invention are explained with reference to drawing 6. In drawing 1 mentioned above, although the phase compensator 50 is established in the exterior of DPLL circuit 12, by this embodiment, the phase compensator 50 is integrated to DPLL circuit 12 and one. That is, since LSI-izing is easy for a DPLL circuit, the phase compensator 50 has composition built in the inside of LSI of DPLL circuit 12.

[0048]The phase comparison inside a DPLL circuit is increasing conventionally the number of the clocks with which phases differ, and its method which brings forward the standup of received data and falling detection time is common. However, thereby, the clock signal generated in a polyphase clock generation part also increases. Therefore, it is necessary to take into consideration the influence of the noise by clock signals, such as a cross talk which receives to other signals of clock wiring.

[0049]On the other hand, the phase compensator of this invention which carries out phase shift amendment by asynchronous is simple for circuitry, and since the phase shift by asynchronous is amended before a received data signal is sent to an internal phase-comparison part, the increase in the different number of clock signals of a phase can be controlled.

[0050]Although the above explained the case where a reset signal was used, a reset signal is not required when you do not need initialization of a circuit.

[0051]In relation to the statement of a claim, this invention can take the following mode further.

[0052](1) The synchronous control system according to any one of claims 1 to 6, wherein the reset signal which synchronizes with said internal clock among the data rows which constitute said received data is inputted and operation of said DPLL circuit is initialized by this reset signal.

[0053](2) The synchronous control system according to any one of claims 1 to 6, wherein said received data are the data from which the data based on a lightwave signal was changed into the electrical signal.

[0054]

[Effect of the Invention]As explained above, in this invention, the phase shift by asynchronous is amended before retiming.

Therefore, in order to perform a phase comparison only to the phase shift by a jitter at the time of retiming, level-luffing-motion time can be shortened and it is effective in the ability to control the digital error of the head part of received data.

It is not necessary to provide the function for obtaining to shortening of the extreme level-luffing-motion time especially by improvement in the speed in the inside of a DPLL circuit, and is effective in the ability to prevent complication of the circuitry of a DPLL circuit by providing before retiming the function which amends a phase.

[Translation done.]

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## TECHNICAL FIELD

[Field of the Invention]Especially this invention relates to the synchronous control system which has a DPLL circuit which synchronizes with an internal clock the received data received from the outside about a synchronous control system.

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## PRIOR ART

[Description of the Prior Art]The data level luffing motion of the burst data receiving system using the timing sampling procedure by the DPLL (Digital Phase Locked Loop) circuit in conventional technology is explained. The composition of an example of the synchronous control system by conventional technology is shown in drawing 7. If the figure is referred to, in the conventional synchronous control system, it is constituted including the light / electrical conversion circuit 4 (it abbreviates to an O/E conversion circuit hereafter) which changes an optical reception signal into an electrical signal, and DPLL circuit 12 which synchronizes the electrical signal after this conversion with a reference clock. And the optical reception signal input terminal 1 and the reset signal input terminal 2 are respectively connected to the input of the O/E conversion circuit 4, and the output, the reset signal input terminal 2, and the reference clock input terminal 3 of the O/E conversion circuit 4 are respectively connected to the input of DPLL circuit 12. The output clock of DPLL circuit 12 is connected to the output clock terminal 13, and data output is connected to the data output terminal 14.
[0003]DPLL circuit 12 has two or more kinds of counting-down circuits inside.
It is a circuit which chooses and uses two or more of these counting-down circuits, and constitutes well-known PLL.
By constituting PLL, retiming processing which synchronizes the signal inputted with a reference clock is performed.
[0004]The timing chart of the synchronous control system of drawing 7 of operation is shown in drawing 8. Here, a reset input signal and a reference clock signal shall be in a synchronous state, and the optical reception signal and reset input signal which are inputted shall have them in an asynchronous state. The Motonobu item received shall be the composition that the preamble data P is added to the head of burst data.
[0005]First, the Motonobu item inputted into the optical received input terminal 1 is changed and outputted to an electrical signal in the O/E conversion circuit 4. In the figure, the inputted

preamble data P of the Motonobu item is expressed as "A", "B", "C", and "D", and data required after this preamble data P is added.

[0006]Here, in order to identify the data transmitted in the state of a gear-tooth omission, it is necessary to initialize a circuit by a non-signal state. For this reason, the reset signal is given between the burst data row and the burst data row. In this case, the time interval of data rows is beforehand measured at the time of initial setting of a system, and the cycle of a reset signal is determined based on this measurement result. By carrying out like this, a data row and a reset signal do not lap, and timing adjustment is made so that a reset signal may exist between data rows.

[0007]The internal reference clock signal of a reception side circuit is inputted into the reference clock input terminal 3. In order to take the synchronization of the electrical signal acquired from the O/E conversion circuit 4, in DPLL circuit 12, the phase comparison of a data signal and a reference clock signal is performed. By choosing the counting-down circuit that this phase comparison result becomes zero, the data output in sync with an output clock and this as shown in the figure is obtained.

[0008]Here, the phase comparison in DPLL circuit 12 is performed as follows. That is, from the reference clock signal inputted, the clock signal with which several kinds of phases differ is generated, and abundance detection of the phase relation of this clock signal and input data signal is carried out. And discernment of data chooses most the clock signal of the phase performed correctly. Retiming of the data is pierced and carried out with this selected clock. Time until a clock signal is chosen from this phase-comparison start draws, and it becomes time.

[0009]Data is not normally identified until operation is stabilized from this level-luffing-motion start, but the signal mistaken in the output terminal of DPLL circuit 12 is outputted. If it is not completed by this state by within a time [ equivalent to the preamble data P ] as the whole receiving system, a digital error will occur in the data head part 120 (shadow area). When the phase comparison of the signal which the jitter has generated in the waveform after a light-receiving level is dramatically small and changes into an electrical signal is performed, this level-luffing-motion time tends to increase. The level-luffing-motion time produced at the time of this phase comparison can be divided roughly into time to adjust an asynchronous phase shift state and time to adjust the phase shift by a jitter.

[0010]As for a DPLL circuit, when a phase comparison becomes difficult and performs high-speed burst data communications so that access speed becomes high-speed, it is indispensable to perform level luffing motion at high speed. Therefore, inside a DPLL circuit, the circuitry of the phase comparison circuit which performs a phase comparison is complicated dramatically.

[Translation done.]

## EFFECT OF THE INVENTION

[Effect of the Invention]As explained above, in this invention, the phase shift by asynchronous is amended before retiming.
Therefore, in order to perform a phase comparison only to the phase shift by a jitter at the time of retiming, level-luffing-motion time can be shortened and it is effective in the ability to control the digital error of the head part of received data.
It is not necessary to provide the function for obtaining to shortening of the extreme level-luffing-motion time especially by improvement in the speed in the inside of a DPLL circuit, and is effective in the ability to prevent complication of the circuitry of a DPLL circuit by providing before retiming the function which amends a phase.

[Translation done.]

## TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]It takes time to choose the clock of a phase with which it mentions above and discernment of data is correctly performed in conventional technology at the time of a phase comparison. It is remarkable about the signal which contained the jitter especially. As a result, if not completed by level-luffing-motion time by within a time [ equivalent to preamble data ], the head of data will start a digital error, and there is a fault of becoming erroneous transmission.

[0012]Time is required, in order for the time of one cycle to become short, and for the rate of the field which a jitter generates to also increase to an eye pattern and to identify data correctly, if access speed increases. Therefore, it becomes the circuitry which incorporated the policy which level-luffing-motion time does not increase. In this case, there is a fault that it is difficult to shorten this level luffing motion, and the circuitry inside DPLL is complicated, so that access speed becomes high-speed.

[0013]The art of shortening the phase level-luffing-motion time in a DPLL circuit also to JP,2-156726,A is indicated. This saves the operation data of the former synchronous state, is setting this as CPU and shortens the synchronous stabilization time at the time of the return after a fault occurrence. However, in this conventional technology, about the signal having contained the jitter, time for discernment of data to choose the clock of the phase performed correctly is taken, and cannot solve the fault mentioned above. To JP,61-240732,A, the rising characteristic (response) of the reference oscillator (crystal oscillator) of a power up is supervised, and the art of controlling and drawing the phase step width of PLL by adding a sampling circuit and an arithmetic circuit, and shortening time is indicated to it. However, about the signal which contained the jitter also in this conventional technology, it is not taken into consideration at all and, similarly the fault mentioned above cannot be solved.

[0014]Also in the burst data communications in which it was made in order that this invention might solve the fault of the conventional technology mentioned above, and the purpose

contained the jitter at high speed, It is providing the synchronous control system which can oppress the increase in level-luffing-motion time, and can prevent digital-error generating of a head part, and also can prevent complication of a DPLL circuit.

[Translation done.]

## MEANS

[Means for Solving the Problem]A synchronous control system by this invention is a synchronous control system which has a DPLL circuit which synchronizes with an internal clock received data received from the outside, It has the phase compensator which amends a phase shift of data which should be inputted into said DPLL circuit, data after this phase shift amendment is inputted into said DPLL circuit, and it was made to perform phase simulation level luffing motion. A capacitative element by which only time when said voltage converting means is equivalent to said phase contrast is charged, A peak detector which detects a peak value of charge voltages of this capacitative element, and a sample hold circuit which samples and holds this peak value with sampling clocks in sync with said clock are included, A time delay of said delay means was controlled according to output voltage of this sample hold circuit. Said phase compensator includes a voltage converting means which changes phase contrast of said received data and said internal clock into voltage, and a delay means which a time delay is controlled [ delay means ] according to this changed voltage, and delays said received data. Said delay means includes a delay circuit which has a time delay equivalent to conversion process time by said voltage converting means, and an integration circuit which integrates with said received data with a damping time constant controlled according to voltage changed by said voltage converting means. Said integration circuit contains a capacitative element in which an electric charge is accumulated by voltage changed by said voltage converting means, and a resistance element which constitutes a time constant circuit with this capacitative element.

[0016]In short, this system has the phase compensator which amends a phase shift by asynchronous. This phase compensator detects a phase shift of a reset input signal and a received data signal, and it delays a received data signal so that that phase shift can be amended. Phase compensator is provided between an O/E conversion circuit and a DPLL circuit, and it has composition which amends a phase before an input of a DPLL circuit.

[0017]Phase compensator provided between an O/E conversion circuit and a DPLL circuit is a circuit which adjusts and amends an asynchronous phase shift state, it is passing through this circuit, and a phase shift of a data signal and a reset input signal which are inputted into a DPLL circuit is amended. Thereby, before being inputted into a DPLL circuit, a synchronization with a received data signal, a reference clock signal, and a reset signal can be taken, and a phase comparison for mainly amending a phase shift by a jitter is performed in a DPLL circuit. Inside a DPLL circuit, a function in particular for shortening level-luffing-motion time extremely is not needed.

[0018]

[Embodiment of the Invention]Next, one gestalt of operation of this invention is explained with reference to drawings. In each figure referred to in the following explanation, identical codes are given to other figures and equivalent portions.

[0019]Drawing 1 is a block diagram showing one gestalt of operation of the synchronous control system by this invention. When the figure is referred to, the point that this system differs from the system of drawing 7 is a point that the phase compensator 50 is formed between the O/E conversion circuit 4 and DPLL circuit 12. That is, in this system, the optical reception signal input terminal 1 and the reset signal input terminal 2 are respectively connected to the input of the O/E conversion circuit 4, and the output, the reset signal input terminal 2, and the reference clock input terminal 3 of the O/E conversion circuit 4 are connected to the input of the complementary positive circuit 50 at least for each. And the output, the reset signal input terminal 2, and the reference clock input terminal 3 of the phase compensator 50 are respectively connected to the input of DPLL circuit 12. The output clock of DPLL circuit 12 is connected to the output clock terminal 13, and data output is connected to the data output terminal 14.

[0020]Next, operation of this system is explained, also referring to the time chart of drawing 2. Here, a reset signal and a reference clock signal shall be in a synchronous state, and the optical reception signal and reset signal which are inputted shall have them in an asynchronous state. The Motonobu item received shall be the composition that the preamble data P is added to the head of burst data.

[0021]First, the Motonobu item inputted into the optical received input terminal 1 is changed and outputted to an electrical signal in the O/E conversion circuit 4. In the figure, the inputted preamble data P of the Motonobu item is expressed as "A", "B", "C", and "D", and data required after this preamble data P is added.

[0022]Here, in order to identify the data transmitted in the state of a gear-tooth omission, it is necessary to initialize a circuit by a non-signal state. For this reason, the reset signal is given from the reset input terminal 2 between the burst data row and the burst data row. Having carried out point ** of the cycle of this reset signal is determined.

[0023]The internal reference clock signal of a reception side circuit is inputted into the reference clock input terminal 3.

[0024]First, in the O/E conversion circuit 4, the inputted optical reception signal is inputted into the phase compensator 50, light / after electrical conversion is carried out. And a delaying amount required of phase compensator 50 inside in order to detect the phase shift quantity by asynchronous [ of a received data signal and a reset signal ] and to double the phase shifted is detected, and it gives the input signal which was able to obtain delay of the part from the O/E conversion circuit 4. This amends the phase shift by asynchronous [ of the reset signal and received data signal in sync with a reference clock signal ]. The data signal which passed through the phase compensator 50 is inputted into DPLL circuit 12, and a phase comparison with a reference clock signal is performed.

[0025]Here, the phase comparison in DPLL circuit 12 is performed as follows as usual. That is, from the reference clock signal inputted, the clock signal with which several kinds of phases differ is generated, and abundance detection of the phase relation of this clock signal and an input data signal is carried out. And discernment of data chooses most the clock signal of the phase performed correctly. Time until a clock signal is chosen from this phase-comparison start draws, and it becomes time.

[0026]In the time of this phase comparison, beforehand, since the phase shift by asynchronous is amended, comparison for mainly amending only the phase shift by a jitter is performed. Therefore, the time required in order to perform this phase correction and to carry out synchronous level luffing motion changes with jitter amounts. In drawing 2, the example which level luffing motion completed to within a time [ which is equivalent to "A" and "B" of the data head part 120 (shadow area) among the preamble data P ] is shown.

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[Translation done.]

* NOTICES *



1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EXAMPLE

[Example]Next, the example of this invention is described with reference to drawing 3. In the figure, the phase compensator 50 is constituted including the asynchronous phase shift detector circuit 6, the delaying amount/DC conversion circuit 10, the DC/DC converter 9, the sampling/hold circuit 8, the DC / delaying amount conversion circuit 7, and the delay circuit 5.
[0028]In the figure, the reset signal input terminal 2 is respectively connected to the reset input of the O/E conversion circuit 4, the asynchronous phase shift detector circuit 6, and DPLL circuit 12, and the reference clock terminal 3 is respectively connected to the clocked into of the asynchronous phase shift detector circuit 6 and DPLL circuit 12.
[0029]Next, the optical reception signal input terminal 1 is connected to the input of the O/E conversion circuit 4, the output of the O/E conversion circuit 4 is connected to the input of the delay circuit 5 and the asynchronous phase shift detector circuit 6, and the output of the delay circuit 5 is connected to the input of DC / delaying amount conversion circuit 7. The output of the asynchronous phase shift detector circuit 6 is connected to the input of a delaying amount / DC conversion circuit 10, and the output of the delaying amount / DC conversion circuit 10 is connected to the input of the DC/DC converter 9. The output of the DC/DC converter 9 is inputted into a sampling / hold circuit 8, and the output of the sampling / hold circuit 8 is connected to the control input of DC / delaying amount conversion circuit 7.
[0030]Here, the control signal output of the asynchronous phase shift detector circuit 6 is connected to the sampling-clocks input of a sampling / hold circuit 8. The output of DC / delaying amount conversion circuit 7 is connected to the input of DPLL circuit 12. The output clock of DPLL circuit 12 is connected to the output clock terminal 13, and the data output of DPLL circuit 12 is connected to the data output terminal 14.
[0031]The more detailed composition of each part of the asynchronous phase shift detector circuit 6 in drawing 3, the delaying amount/DC conversion circuit 10, and the DC / delaying amount conversion circuit 7 is shown in drawing 4. As shown in drawing 4 the asynchronous

phase shift detector circuit 6, The monostable multivibrator circuit (it is hereafter called a monomulti vibrator circuit) 32 for detecting the standup position of a preamble data signal, It is constituted including the inverter 40 and the monomulti vibrator circuit 35 for detecting the falling position of a reset signal (b). Between the power supply 38 and the ground 34, the resistance element 39 and the capacitative element 33 are formed, and the output pulse width of the monomulti vibrator circuit 32 is determined with these elements. Similarly, between the power supply 42 and the ground 37, the resistance element 43 and the capacitative element 36 are formed, and the output pulse width of the monomulti vibrator circuit 35 is determined with these elements.

[0032]The inverter 31 with which the asynchronous phase shift detector circuit 6 reverses the output of the monomulti vibrator circuit 32, AND circuit 30 which takes the logical product of this inverted output and the output of the monomulti vibrator circuit 35, This logical product output consists of standups of the reference clock including NOR circuit 28 which considers the D-flip-flop circuit 29, and this reversal Q output and the logical product output of AND circuit 30 as an input.

[0033]The delaying amount / DC conversion circuit 10 is constituted including the capacitative element 26 charged with the output of NOR circuit 28, and the peak detector 25 which detects the peak voltage by charge of this capacitative element 26. 27 is a ground.

[0034]The inverter 20 with which DC / delaying amount conversion circuit 7 was formed in the input stage, It is constituted including the inverter 23 formed in the output stage, the resistance element 45 and the capacitative element 21 which constitute an integration circuit, and the resistance 24 for charging the capacitative element 21 with the output of a sampling/hold circuit. 22 is a ground.

[0035]Operation of each part of drawing 4 is shown in the time chart of drawing 5. In drawing 5, the waveform of the portion of numerals (a) - (j) attached in drawing 4 is shown.

[0036]Here, a reset signal (b) and a reference clock signal (c) shall be in a synchronous state, and the optical input signal (a) and reset signal (b) to receive shall have them in an asynchronous state. As for the composition of the Motonobu item which receives, the preamble data P shall be added to the head of burst data.

[0037]First, the Motonobu item inputted into the optical received input terminal 1 is changed into an electrical signal in the O/E conversion circuit 4. Here, in a figure, the inputted preamble data of the Motonobu item shall be expressed as "A", "B", "C" and "E", "F", and "G", and data required after this preamble data shall be added.

[0038]In order to identify the data transmitted in the state of a gear-tooth omission, it is necessary to initialize a circuit by a non-signal state. For this reason, between a burst data row and a burst data row, a reset signal (b) is given from the reset input terminal 2. The reference clock signal (c) of a receiver is inputted into the reference clock input terminal 3.

[0039]In the O/E conversion circuit 4, the received optical data signal (a) is inputted into the phase compensator 50, light / after electrical conversion is carried out. In the asynchronous phase shift detector circuit 6 of phase compensator 50 inside, the standup position of a preamble data signal and the falling position of a reset signal (b) are respectively detected using the monomulti vibrator circuits 32 and 35. The result of having detected the standup position of the preamble data signal is reversed, and a logical product is taken with the result and AND circuit 30 which detected the falling position of the reset signal. It uses as sampling clocks (g) which mention this signal later.

[0040]As a result of detecting the period from the falling position of this reset signal until a preamble data signal rises, it is processed by the D-flip-flop circuit 29 and NOR circuit 28. The signal for detecting time until the standup of a reference clock signal (c) comes from the standup of a preamble data signal by carrying out like this is acquired.

[0041]Here, the detected time serves as phase shift quantity by asynchronous, and it becomes a delaying amount for amending a phase. This signal is told to the delaying amount / DC conversion circuit 10 of the next step. In a delaying amount / DC conversion circuit 10, the capacitative element 26 is charged with the output signal of the asynchronous phase shift detector circuit 6, and the peak value of these charge voltages (d) is detected in the peak detection circuit 25. In this case, since full charge of the capacitative element 26 is carried out when phase shift quantity is large, the peak value of charge voltages (d) becomes large. On the contrary, when phase shift quantity is small, full charge of the capacitative element 26 is not carried out, but the peak value of charge voltages (d) becomes small. Thus, the delaying amount for amending a phase is changed into the DC voltage of V1 and V2 by detecting a peak value. This changed DC signal is an output signal (e) of a delaying amount / DC conversion circuit 10.

[0042]Next, with the DC/DC converter 9, a DC signal is increased N times and turns into a signal (f) of V1xN and V2xN. Thus, increasing N times, the output signal (e) of a delaying amount / DC conversion circuit 10 is a minute pressure value.

It is for using a pressure value required to give an electric charge to the capacitative element 21 mentioned later.

[0043]In a sampling / hold circuit 8, the sampling clocks (g) outputted from the asynchronous phase shift detector circuit 6 perform sampling/hold operation of a signal (f). And between 1 bursts, the sampled DC signal is held and is stabilized. A DC signal (h) is outputted from this sampling / hold circuit 8. Sampling clocks (g) are signals which change whenever a burst signal is inputted.

[0044]Using the DC signal (h) outputted from a sampling / hold circuit 8, by DC / delaying amount conversion circuit 7, an electric charge is given to the capacitative element 21 and the

standup of an input signal and falling are adjusted to the threshold of the inverter circuit 23. You make it delayed by carrying out like this so that the phase shift according the input signal inputted via the delay circuit 5 to asynchronous may be amended. Thereby, a data signal (j) is outputted from DC / delaying amount conversion circuit 7.

[0045]Here, the delaying amount of the delay circuit 5 is set as the amount of absolute delay in the asynchronous phase shift detector circuit 6, the delaying amount/DC conversion circuit 10, the DC/DC converter 9, and the sampling/hold circuit 8. That is, the phase contrast of an optical data signal (a) and data signal (i) after delay by the delay circuit 5 is equivalent to the delaying amount.

[0046]The data signal (j) acquired from DC / delaying amount conversion circuit 7, After being inputted into DPLL circuit 12, the result of having performed the phase comparison of a preamble data signal and a reference clock signal, and having performed retiming to the output clock terminal 13 and the data output terminal 14 is obtained as usual using the clock with which several kinds of phases differ.

[0047]Next, other gestalten of operation of this invention are explained with reference to drawing 6. In drawing 1 mentioned above, although the phase compensator 50 is established in the exterior of DPLL circuit 12, by this embodiment, the phase compensator 50 is integrated to DPLL circuit 12 and one. That is, since LSI-izing is easy for a DPLL circuit, the phase compensator 50 has composition built in the inside of LSI of DPLL circuit 12.

[0048]The phase comparison inside a DPLL circuit is increasing conventionally the number of the clocks with which phases differ, and its method which brings forward the standup of received data and falling detection time is common. However, thereby, the clock signal generated in a polyphase clock generation part also increases. Therefore, it is necessary to take into consideration the influence of the noise by clock signals, such as a cross talk which receives to other signals of clock wiring.

[0049]On the other hand, the phase compensator of this invention which carries out phase shift amendment by asynchronous is simple for circuitry, and since the phase shift by asynchronous is amended before a received data signal is sent to an internal phase-comparison part, the increase in the different number of clock signals of a phase can be controlled.

[0050]Although the above explained the case where a reset signal was used, a reset signal is not required when you do not need initialization of a circuit.

[0051]In relation to the statement of a claim, this invention can take the following mode further.

[0052](1) The synchronous control system according to any one of claims 1 to 6, wherein the reset signal which synchronizes with said internal clock among the data rows which constitute said received data is inputted and operation of said DPLL circuit is initialized by this reset signal.

[0053](2) The synchronous control system according to any one of claims 1 to 6, wherein said

received data are the data from which the data based on a lightwave signal was changed into the electrical signal.

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[Translation done.]

## DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a block diagram showing the composition of the synchronous control system by one gestalt of operation of this invention.
[Drawing 2]It is a time chart which shows operation of the synchronous control system of drawing 1.
[Drawing 3]It is a block diagram showing the example of an internal configuration of the phase compensator in drawing 1.
[Drawing 4]It is a block diagram showing the more detailed example of an internal configuration of the phase compensator in drawing 1.
[Drawing 5]It is a time chart which shows operation of each part of drawing 4.
[Drawing 6]It is a block diagram showing the composition of the synchronous control system by other gestalten of operation of this invention.
[Drawing 7]It is a block diagram showing the composition of the conventional synchronous control system.
[Drawing 8]It is a time chart which shows operation of the synchronous control system of drawing 7.
[Description of Notations]
1 Optical reception signal input terminal
2 Reset signal input terminal
3 Reference clock input terminal 3
4 Light / electrical conversion circuit
5 Delay circuit
6 Asynchronous phase shift detector circuit
7 DC / delaying amount conversion circuit
8 A sampling/hold circuit

9 DC/DC converter
10 A delaying amount/DC conversion circuit
12 DPLL circuit
13 Output clock terminal
14 Data output terminal
50 Phase compensator

[Translation done.]